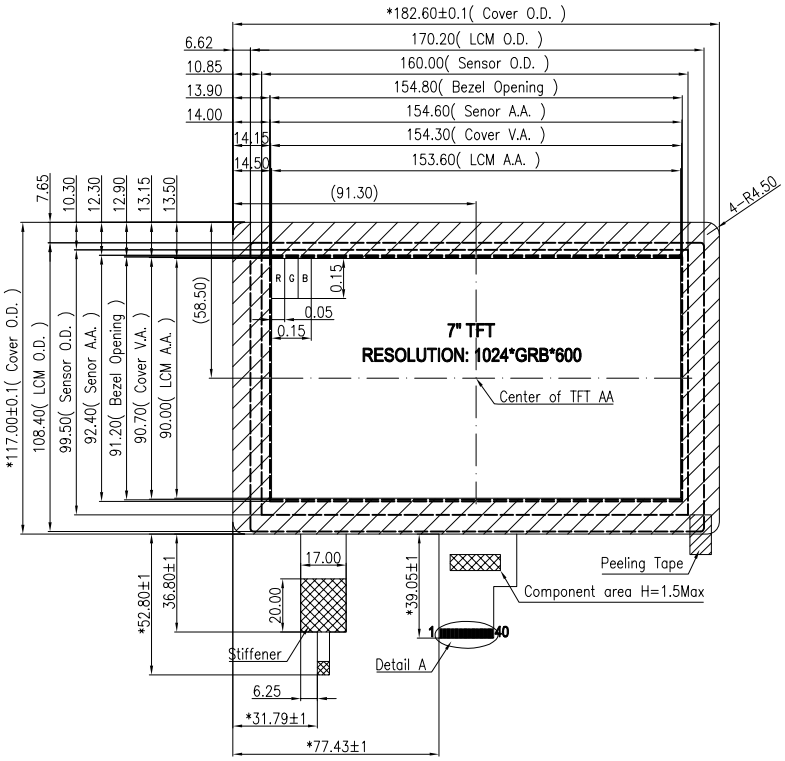
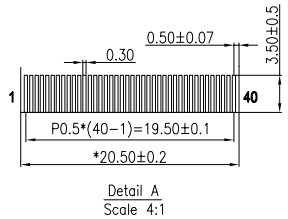
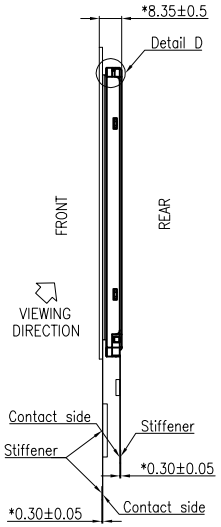
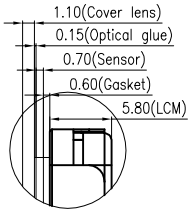


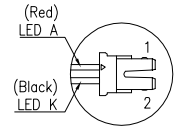


Detail A
Scale 4:1



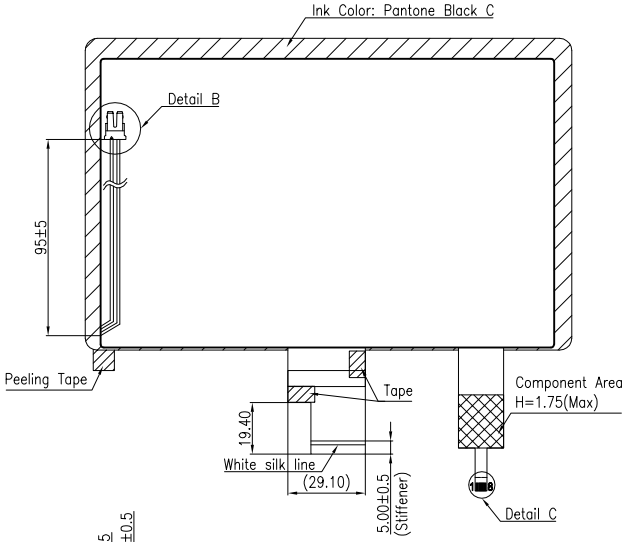


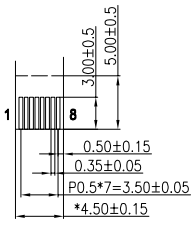
Detail D
Scale 4:1



Mating connector: JST SM02B-BHSS-1-TB or equivalent

Detail B
Scale 2:1





Detail C
Scale 4:1

CTP (I²C) PIN FUNCTION

Pin No.	Symbol	Description
1	VDD1	Power,VDD1=3.3V(type)
2	GND	Ground
3	RST	Reset,active high
4	SCL	I²C Clock input
5	SDA	I²C Data signal
6	INT	Interrput output
7	NC	No Connect
8	NC	No Connect

REVISIONS							DRAWN	CHECK	APPROVE	PART NO.	JYG-102460004G(R)-KT0L2-VF		
MARK	DATE	DESCRIPTION	DRAWN	CHECK	APPROVE	NAME	LIChangxing			DWG NO.	G102460004G(R)-WX-VF		
										SUB-DWG NO.	4		
						DATE	2015.4.17			PAGE	1-1	UNIT	mm
						UNLESS OTHERWISE NOTED TOLERANCES : ±0.3				JIYA(LANGFANG) ELECTRONICS CO.,LTD			

Pins Description

Pin No.	Symbol	Description
1	VCOM	Common Voltage
2	VDD	Power Voltage for digital circuit
3	VDD	Power Voltage for digital circuit
4	NC	No connection
5	Reset	Global reset pin
6	STBYB	Standby mode, Normally pulled high STBYB = "1", normal operation STBYB ="0", timing controller, source,driver will turn off, all output are High-Z
7	GND	Ground
8	RXIN0-	-LVDS differential data input
9	RXIN0+	+LVDS differential data input
10	GND	Ground
11	RXIN1-	-LVDS differential data input
12	RXIN1+	+LVDS differential data input
13	GND	Ground
14	RXIN2-	-LVDS differential data input
15	RXIN2+	+LVDS differential data input
16	GND	Ground
17	RXCLKIN-	-LVDS differential clock input
18	RXCLKIN+	+LVDS differential clock input
19	GND	Ground
20	RXIN3-	-LVDS differential data input
21	RXIN3+	+LVDS differential data input
22	GND	Ground
23	NC	No connection
24	NC	No connection
25	GND	Ground
26	NC	No connection
27	DIMO	Backlight CABC controller signal output

Pins Description

Pin No.	Symbol	Description
28	SELB	SELB="0",LVDS input data is 8 bits SELB="1",LVDS input data is 6 bits
29	AVDD	Power for Analog Circuit
30	GND	Ground
31	NC	No connection
32	NC	No connection
33	L/R	Horizontal inversion,L/R="0", set right to left scan direction. When L/R="1", set left to right scan direction.
34	U/D	Vertical inversion,U/D="0", set top to bottom scan direction. When U/D="1", set bottom to top scan direction.
35	VGL	Gate OFF Voltage
36	CABCEN1	When CABC_EN="00", CABC OFF. When CABC_EN="01", user interface image. When CABC_EN="10", still picture. When CABC_EN="11", moving image. When CABC off, don't connect DIMO,else connect it to backlight.
37	CABCEN0	
38	VGH	Gate ON Voltage
39	NC	No connection
40	NC	No connection

NOTE:

1. DISPLAY TYPE: TFT-NEGATIVE-TRANSMISSIVE
2. VIEWING DIRECTION: ALL
3. DRIVE METHOD: 1/600DUTY,VDD=3.3±0.3V
4. OP. TEMP.: -20°C~70°C
5. ST. TEMP.: -30°C~80°C
6. LVDS interface
7. BACKLIGHT:LED COLOR-WHITE,If=120mA, Vf=24.3~30.6V
   LCM LUMINANCE : 680CD/m² (typ.), 540CD/m² (min.)
   Uinformity>70%
8. ROHS
9. CTP IC: PIXCIR Tango-C48
10. LCD DRAWING NO.:JY14A87

REVISIONS							DRAWN	CHECK	APPROVE	PART NO.	JYG-102460004G(R)-KT0L2-VF		
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										SUB-DWG NO.	4		
						DATE	2015.4.17			PAGE	1-2	UNIT	mm
						UNLESS OTHERWISE NOTED TOLERANCES : ±0.3				JIYA(LANGFANG) ELECTRONICS CO.,LTD			

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PRODUCT DRAWING	CUSTOMER DRAWING:	
	FILENAME	TOTAL PAGES: 3
PRODUCT NO. JYG-102460004G(R)-KT0L2-VF	☑ INITIATE ☐ REVISE	ORIGINAL DATE 2015.4.17

REVISIONS

REV	DESCRIPTION	DATE