MT–12864J

LCD display module
graphic 128x64 dots

General description

MT–12864J LCD display module is composed of LSI controller and LCD panel. The display module appearance is shown in Fig. 1. K145ВГ10 controller manufactured by ANGSTREM OJSC (www.angstrem.ru) is an analogue of SAMSUNG KS0108.
Each glowing dot on LCD has its corresponding logic "1" in a RAM cell of the display module. Dimensions of the display module are shown in Fig. 5.
MT–12864J displays are available in 3V and 5V supply voltage versions.

Caution! Exposure of the display module to the static electricity of over 30V must be avoided!

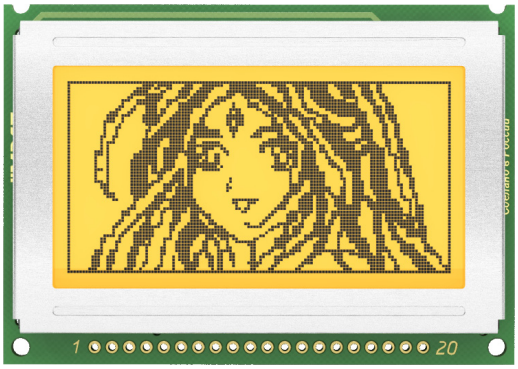


Fig. 1.

Display module features

- receives instructions from the data bus DB7-DB0 (instructions are listed in Table 3);
- read data from RAM to the bus DB7-DB0
- write data in RAM 8-bit data bus DB7-DB0;
- read the status of a condition on the bus DB7-DB0 (instructions are listed in Table 3);
- backlight and contrast adjustment.

Timing diagrams are shown in Fig.3.

Contrast adjustment

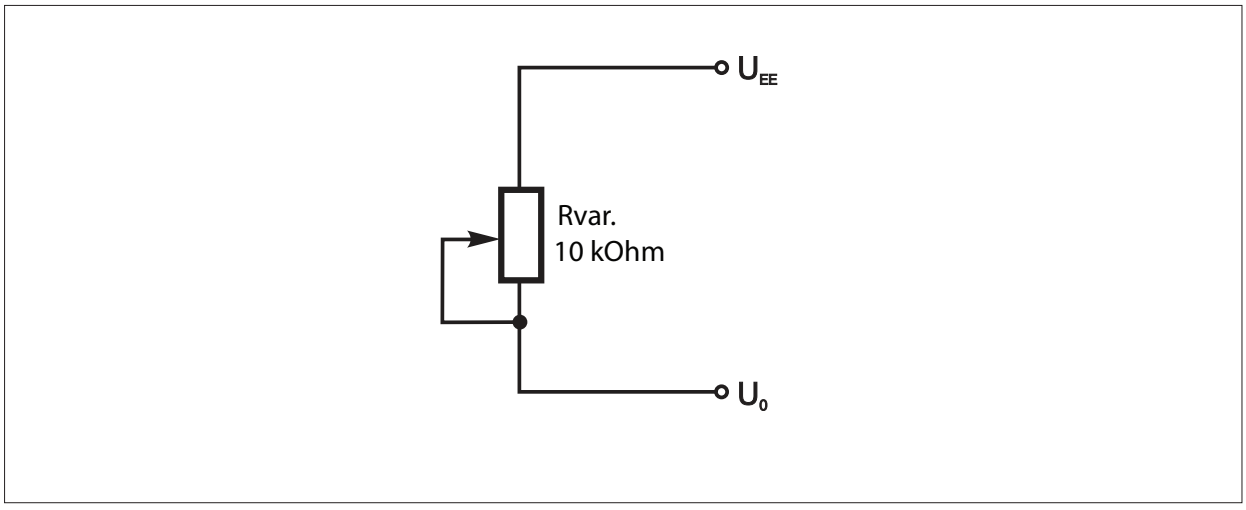


Fig. 2.

Table 1. Dynamic characteristics of the display module.

Item	Symbol	Min.	Max.	Units
Read/Write cycle time	t_{CYCE}	1000	–	ns
Read/write enable pulse duration	PW_{EH}	450	–	ns
Rise/fall time	t_{Er}, t_{Ef}	–	25	ns
Address preset time	t_{AS}	140	–	ns
Address hold time	t_{AH}	10	–	ns
Data output time	t_{DDR}	–	320	ns
Data delay time	t_{DHR}	20	–	ns
Data preset time	t_{DSW}	200	–	ns
Data hold time	t_{H}	10	–	ns
Minimal pause between the filing of commands or data	t_{W}	8	–	μs

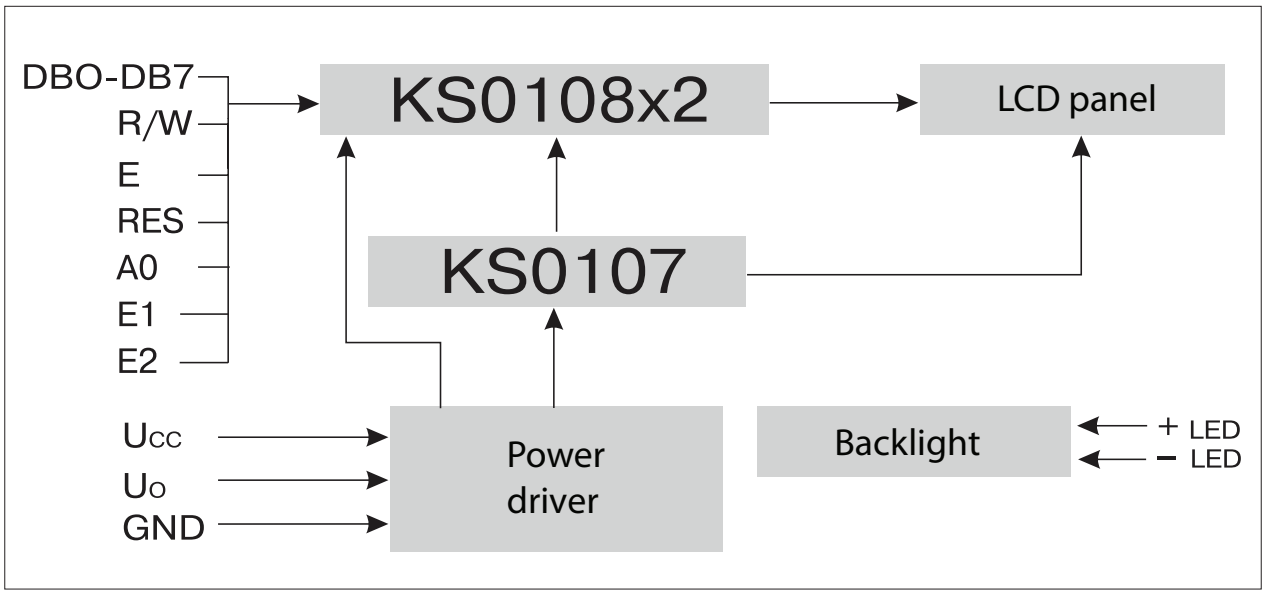
DC characteristics of the display module

Table 2. DC characteristics.

Item		Symbol	Ucc=5V			Ucc=3V			Units
			min.	nom.	max.	min.	nom.	max.	
Supply voltage		U_{CC}	2,8	3,0	3,3	4,5	5,0	5,5	V
Consumption current		I_{CC}	–	4	–	–	4	–	mA
Input “High” Voltage		U_{IH}	2,0	–	U_{CC}	2,0	–	U_{CC}	V
		$U_{IH\ RES*}$	$0,7*U_{CC}$	–	U_{CC}	$0,7*U_{CC}$	–	U_{CC}	V
Input “Low” Voltage		U_{IL}	0	–	0,8	0	–	0,8	V
		$U_{IL\ RES*}$	0	–	$0,3*U_{CC}$	0	–	$0,3*U_{CC}$	V
Output “High” Voltage at I_{OH}=0.2 mA		U_{OH}	2,4	–	–	2,4	–	–	V
Output “Low” Voltage at I_{OL}=1.6 mA		U_{OL}	–	–	0,4	–	–	0,4	V
Backlight current at backlight supply voltage Ucc=5 V	For amber and yellow-green	I_{LED}	–	64	–	–	64	–	mA
	For white and sky-blue	I_{LED}	–	64	–	–	64	–	mA

* input voltage for output RES

Flow chart



Timing diagrams

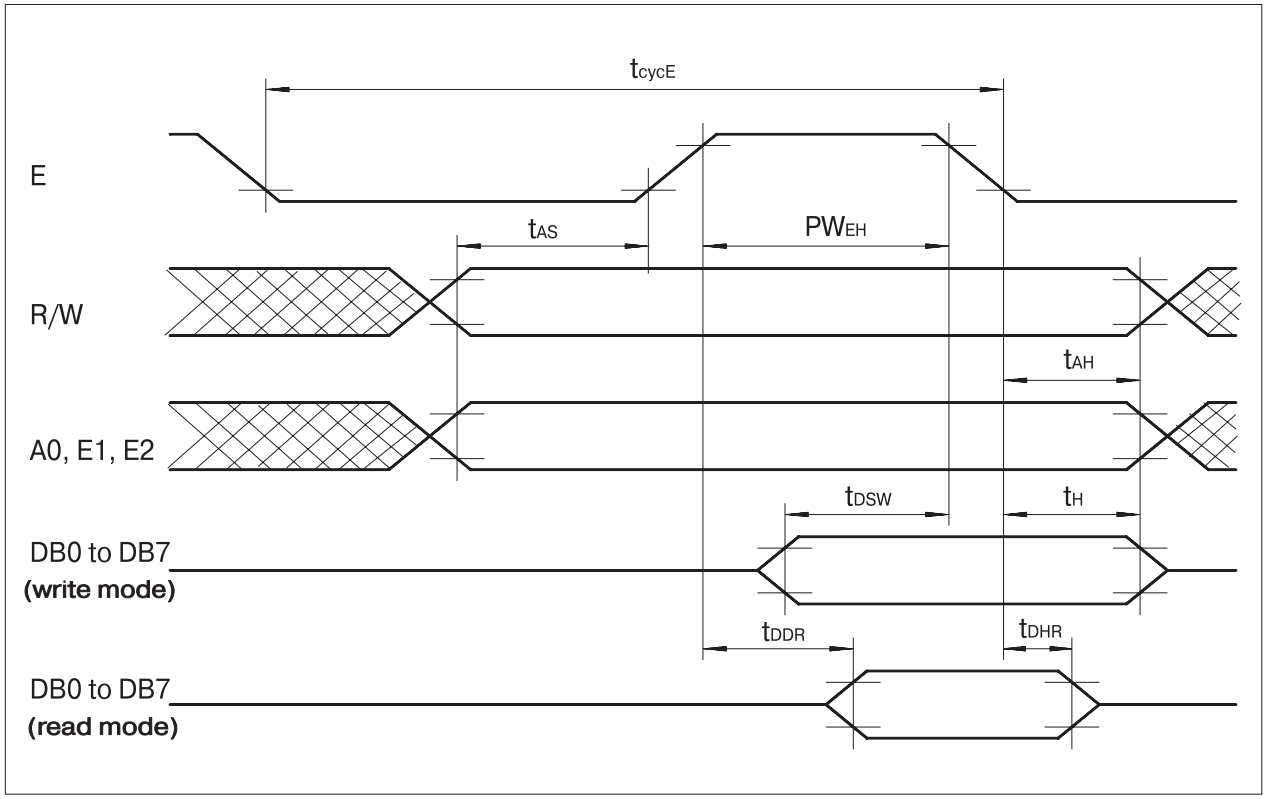


Fig. 3. Time diagrams exchange Protocol

Description of instructions

Table 3.

Instruction	Command code										Function		
	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Display ON/OFF	0	0	0	0	1	1	1	1	1	0/1	Sets LCD on or off, irrespective of the data in display RAM or internal status		
											1	display on	
											0	display off	
Display START Line	0	0	1	1	Display START Line(0...63)						Specifies RAM line to be displayed in the top line of LCD (LCD start line)		
Set Page	0	0	1	0	1	1	1	Page (0...7)			Sets RAM page in the page address mode (page 0...7)		
Set Address	0	0	0	1	Column address (0...63)						Sets RAM column in the column address mode		
Status Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Reads the display status byte		
											BUSY	1	The display module is busy with internal processing
												0	The display module is ready to work with external MP
											ON/OFF	1	LCD if off
												0	LCD is on
											RESET	1	Reset status
												0	Normal status
Write Data to RAM	1	0	Write Data								Write data to the display module RAM		These instructions select RAM at the preset address, whereupon the column address is incremented
Read Data from RAM	1	1	Read Data								Read data from the display module RAM		

Initial setup

For initial setup of the display module it is necessary to send RES signal equal to logic '0' lasting for at least 1 μs. Upon this signal the display module executes 'Display Start Line' (set to 0) and 'DisplayOff' instructions. After RES is deactivated (switchover to logic '1' with front duration of 200 ns max), wait for the 'BUSY' and 'RESET' bits reset in the status register of both crystals or hold at least 10 μs pause. Now the display module will operate normally. Status can be checked even with RES signal being active (= logic '0').

RAM allocation

The display module contains RAM for storing the data displayed on 64x64x2 bits LCD (64x64 bits per crystal). To select the required crystal, E1 and E2 pins are used. RAM is split into 8 pages, 64x8 bits each. Each glowing dot on LCD has its corresponding logic '1' in a display module RAM cell. Correlation between the RAM addresses and the dots displayed on LCD is shown in Fig. 4.

Data reading and writing

Reading (writing) of information from (to) the display module is performed in a per-page method (64x8 bits or 64x1 byte). Each page represents 64 bytes. To read or write a data byte at an arbitrary address, the RAM page and the address inside the RAM page need to be preset. This can be done using the 'Set Page' and 'Set Address' instructions correspondingly. After that the data byte can be read or written.

In the data read mode, after the execution of the 'Set Page' and 'Set Address' instructions, a single 'no-op' read operation should be executed. The result of that operation cannot be used.

The display module supports a continuous sequence of read or write operations: after reading (writing) of one byte the address count increments automatically by 1, and the display module is ready to execute the new read (write) operation at the next address without the need for presetting RAM page and address. The column count counts only within one page! Upon achieving address 63, the next count value will be 0 and so on.
Between any two data (instructions) transmissions, it is necessary to hold at least 8 μs pause or wait for the reset of BUSY flag in the status register of the crystal to be accessed.

Vertical displacement of displayed information

The display module supports the 'Display START Line' instruction that sets the number of the topmost displayed line. The number can be within the range of 0 to 63, which corresponds to the interval from the first line of RAM 0 page to the last line of RAM 7th page. Right after the 7th line, the 0 line will be displayed once again. This enables smooth vertical information shift on LCD through modifying the number of the first displayed line.

RAM allocation

Fig. 4. Correlation between the module RAM addresses and the displayed dots on LCD

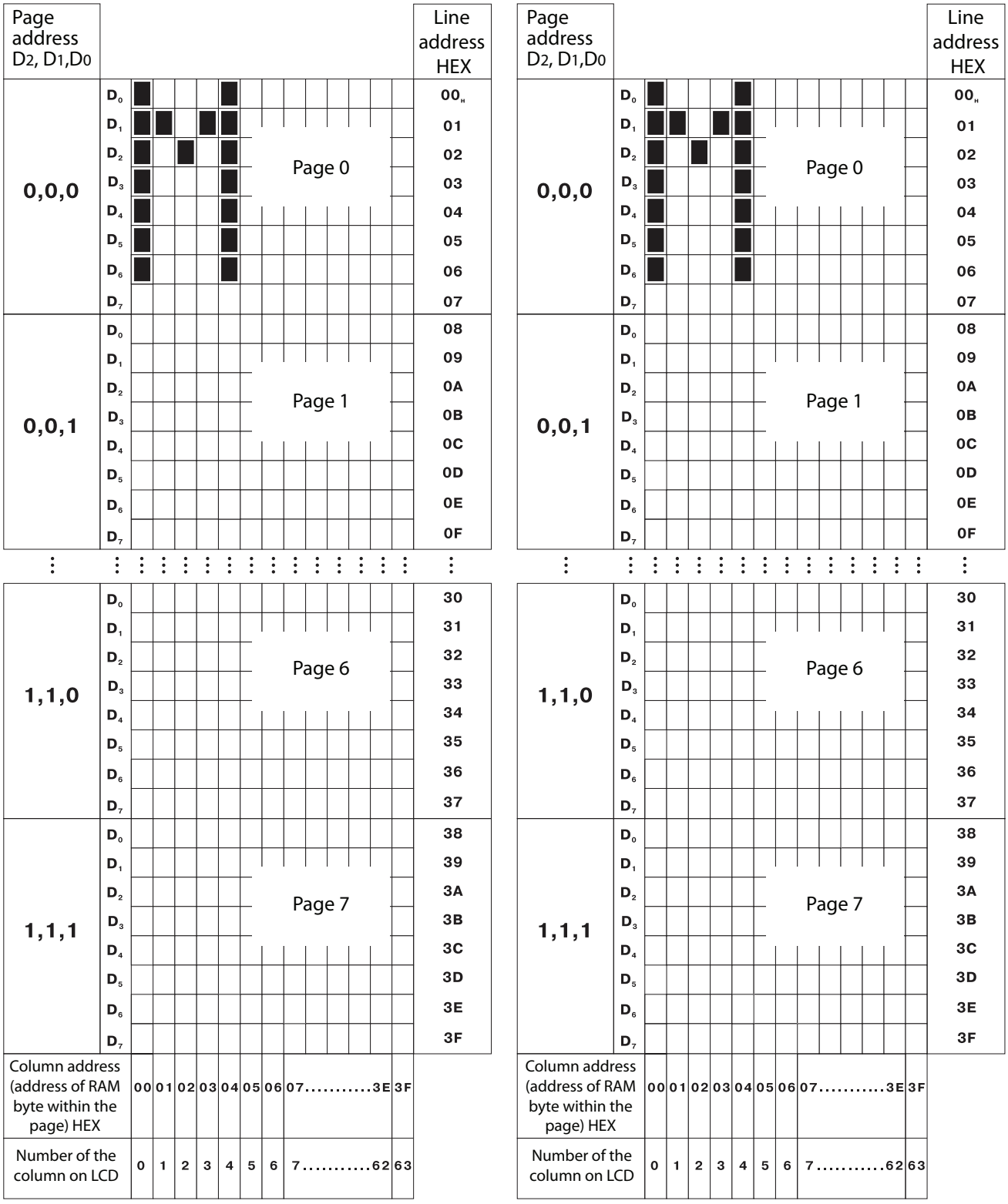


Table 4. Pinout.

Pin	Symbol	Pin assignment
1	GND	Common pin (CP)
2	Ucc	Display module power supply (digital part)
3	U_0	LCD power input
4	A_0	Choice of register data / commands
5	R/W	Read / Write
6	E	Data strobing
7	DB0	Data bus
8	DB1	Data bus
9	DB2	Data bus
10	DB3	Data bus
11	DB4	Data bus
12	DB5	Data bus
13	DB6	Data bus
14	DB7	Data bus
15	E1	Select crystal 1
16	E2	Select crystal 2
17	RES	Initialization
18	U_{EE}	Crystal select
19	K	– of the backlight power supply
20	A	+ of the backlight power supply

LCD display module dimensions

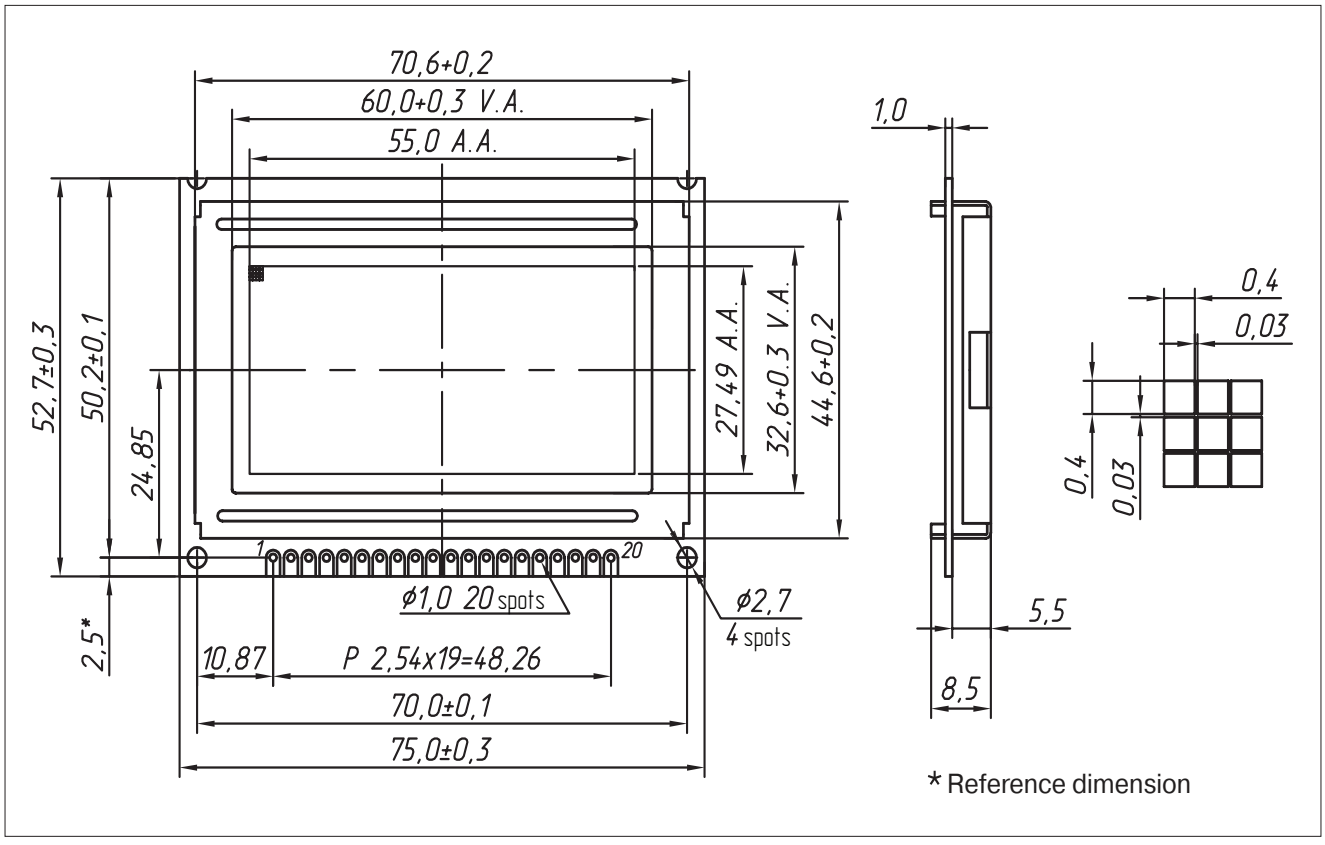


Fig. 5.

Revision history

Document version	Date	Alterations	Page
1.0	09/07/2013	Revision 1	

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