General description

MT–24S2L LCD display module is composed of LSI controller and LCD panel. KB1013VG6 controller manufactured by ANGSTREM OJSC (www.angstrem.ru) is an analogue of HITACHI HD44780 and SAMSUNG KS0066. The display module comes with LED backlight.
MT–24S2L appearance is shown in Fig.1.

Fig. 1

MT–24S2L allows displaying 2 line comprising 24 characters. Characters are displayed in 5x8 dot matrix. Characters are separated by the intervals of 1 displayed dot. Each displayed character is assigned a corresponding code in the display module RAM cell.
The display module incorporates two types of memory (memory for storing codes for displayed characters and memory of the user character-generator) and LCD panel control logic.
The display module dimensions are shown in Figure 7.

Caution! Exposure to static electricity of over 30 V must be avoided.

Display module features

- The display module features two software-switchable pages of a built-in character generator (available alphabets: Russian, Ukrainian, Belorussian, Kazakh, and English; see Tables 5 and 6);
- supports operation on both 8-bit and 4-bit data bus (to be set at initialization);
- receives instructions from the data bus (instructions are listed in Table 4);
- writes data from the data bus to RAM;
- reads data from RAM to the data bus;
- reads status to the data bus (see Table 4);
- stores up to 8 user-defined character patterns;
- returns blinking (or non-blinking) cursor of two types;
- backlight and contrast adjustment.

Product background

The display module is controlled via 4-bit or 8-bit parallel interface.
Timing diagrams are shown in Fig.3 and 4.
Dynamic characteristics are listed in Table 2.
Interface exchange examples are shown in Fig. 5 and 6.
Programmable control is carried out through a set of instructions listed in Table 4.
Prior to operating the display module, initial setting shall be performed.
The built-in character generator is presented in Tables 5 and 6.
The Display module enables setting the patterns for 8 additional characters to be used on an equal basis with the integrated ones. Additional pattern setting is exemplified by Table 3.

Table 1. Dynamic characteristics of the display module.

Item	Symbol	U_{CC}=5V		U_{CC}=3V		Units
		min.	max.	min.	max.	
Read/write cycle time	t_{cycE}	500	–	1000	–	ns
Read/write enable pulse duration	PW_{EH}	230	–	450	–	ns
Rise/fall time	t_{Er}, t_{Ef}	–	20	–	25	ns
Address preset time	t_{AS}	40	–	60	–	ns
Address hold time	t_{AH}	10	–	20	–	ns
Data output time	t_{DDR}	–	120	–	360	ns
Data delay time	t_{DHR}	5	–	5	–	ns
Data preset time	t_{DSW}	80	–	195	–	ns
Data hold time	t_H	10	–	10	–	ns

Contrast Adjustment

In 5V display modules, UO pin should be connected to GND pin, while in 3V displays, UO pin should be left unconnected. For contrast adjustment, an external 10kOhm variable resistor R is used.

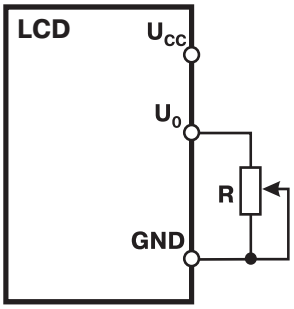


Fig. 2

DC characteristics of the display module

Table 2. DC characteristics.

Item		Symbol	U_{CC}=5V			U_{CC}=3V			Units
			min.	nom.	max.	min.	nom.	max.	
Supply voltage		U_{CC}	4,5	5,0	5,5	2,7	3,0	3,6	V
Consumption current		I_{CC}	–	0,8	1,0	–	0,8	1,0	mA
Input “High” Voltage at I_{IH}=0,1 mA		U_{IH}	2,2	–	U_{CC}	2,2	–	U_{CC}	V
Input “Low” Voltage at I_{IL}=0,1 mA		U_{IL}	–0,3	–	0,6	–0,3	–	0,4	V
Output “High” Voltage at I_{OH}=0,2 mA		U_{OH}	2,4	–	–	2,0	–	–	V
Output “Low” Voltage at I_{OL}=1,2 mA		U_{OL}	–	–	0,4	–	–	0,4	V
Backlight current at backlight supply voltage =U_{CC}	For amber and yellow-green	I_{LED}	–	120	–	–	120	–	mA
	For white and sky-blue	I_{LED}	–	100	–	–	100	–	mA

Timing diagrams

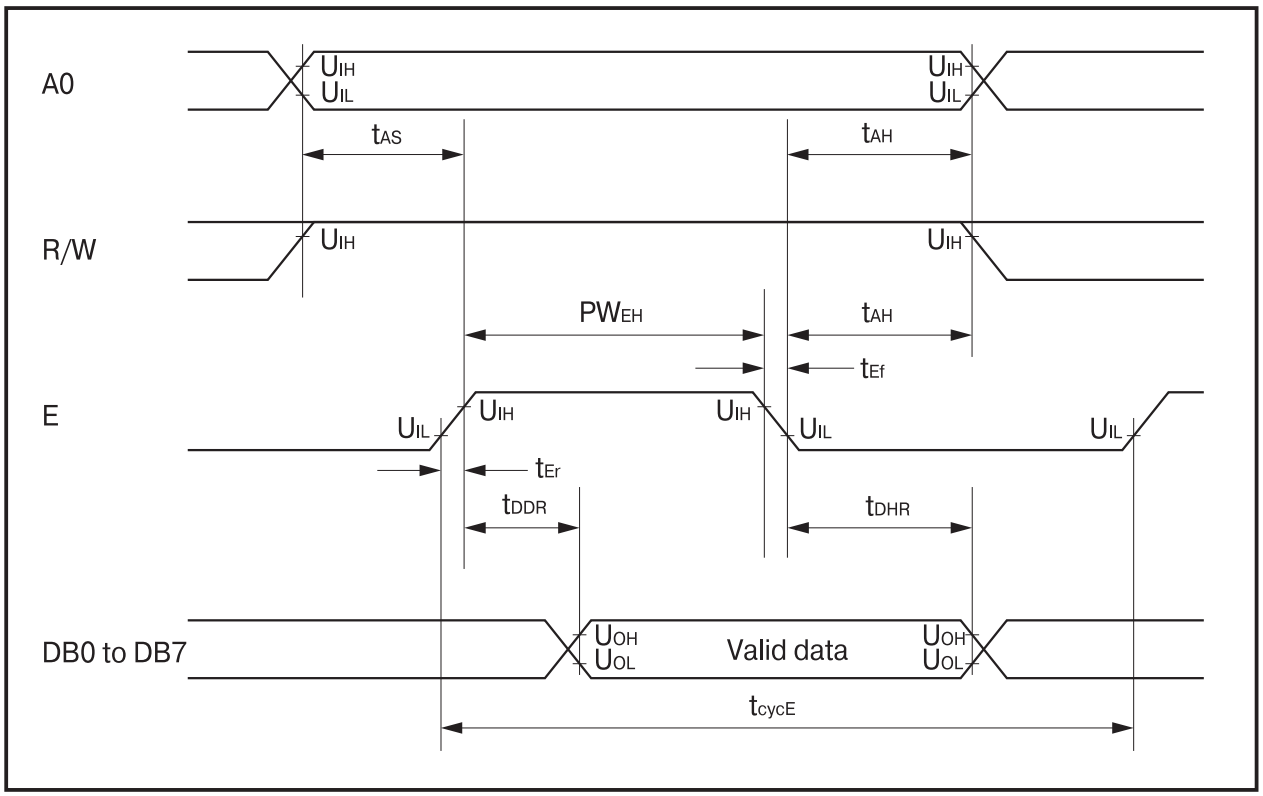


Fig. 3. Read diagram

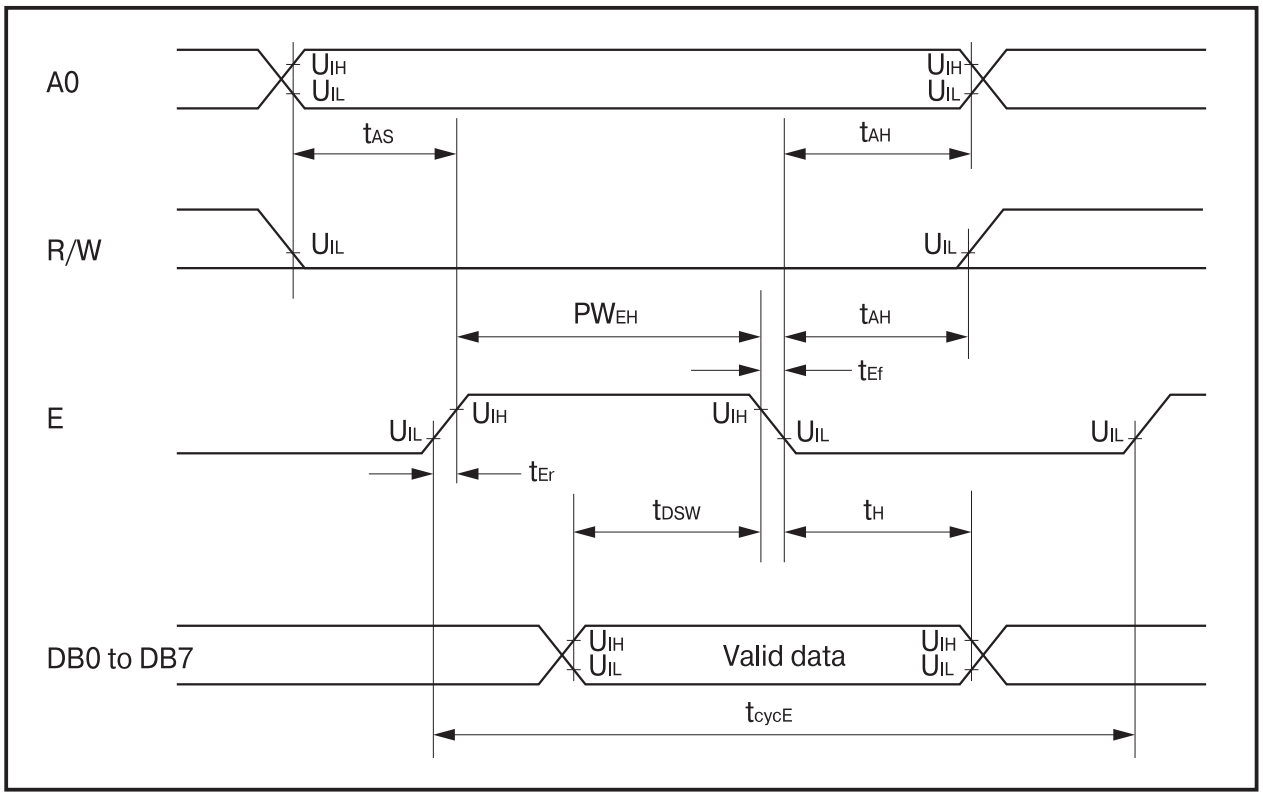


Fig. 4. Write diagram

4-bit interface exchange diagram

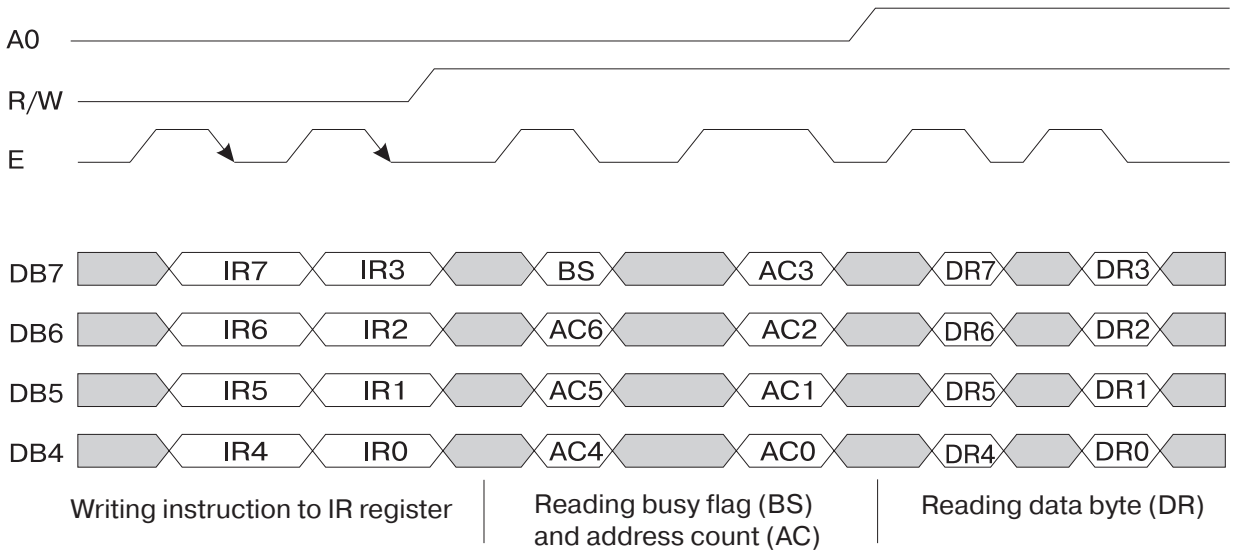


Fig. 5

Note. In each exchange cycle, all 8 bits (two times by 4 bits) should be transmitted (read or written). Transmission of 4 most significant bits (MSB) not followed by the subsequent transmission of 4 least significant bits (LSB) is not permitted.

8-bit interface exchange diagram

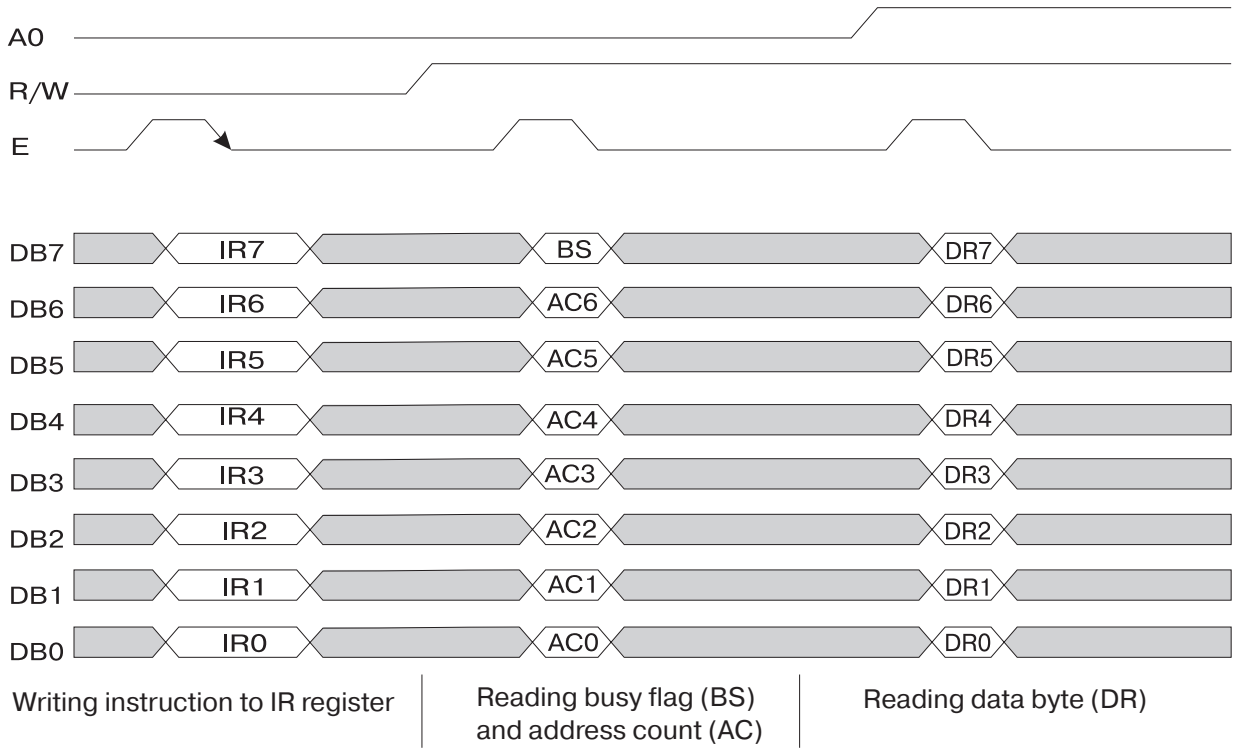
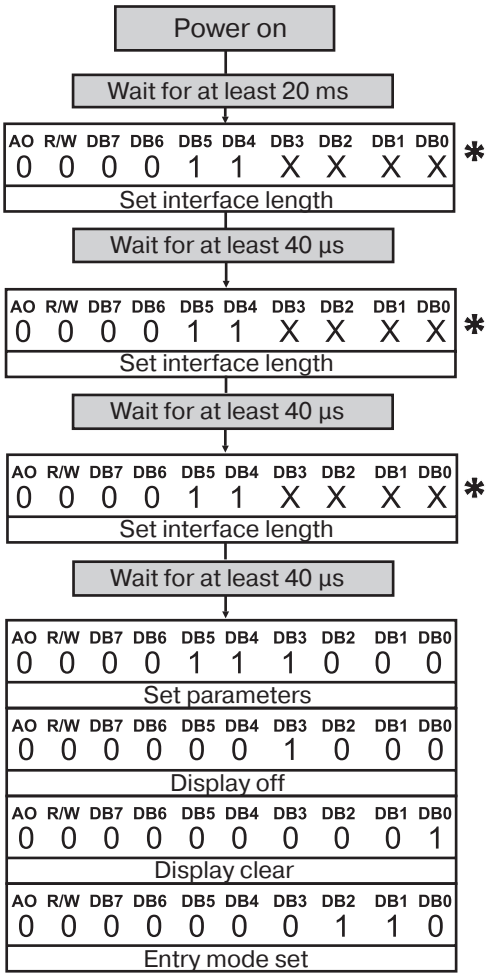


Fig. 6

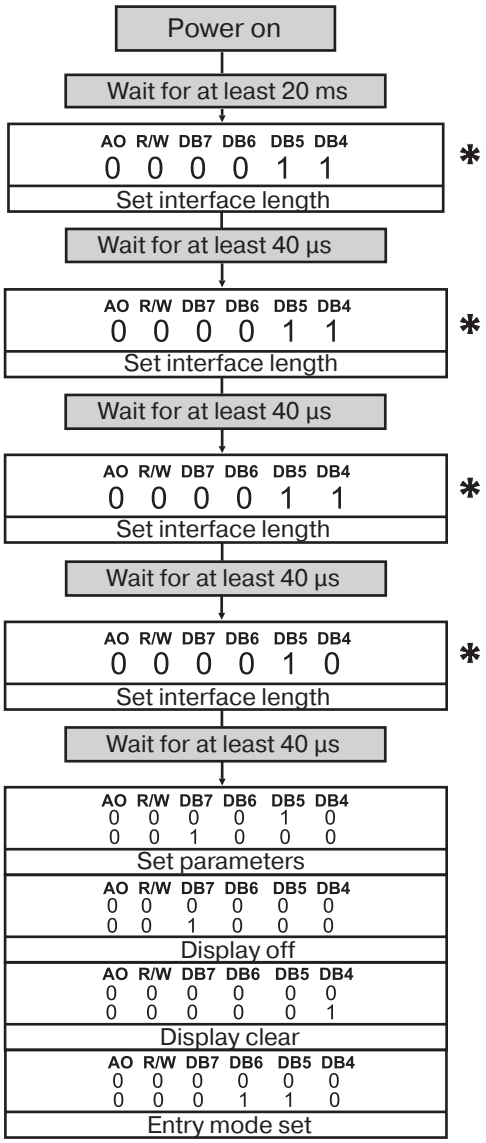
Initial setup

For operating the display module in a normal mode, the following setup instructions should be issued:

8-bit mode of operation



4-bit mode of operation



* — do not check the Busy Flag (BS) after execution of the above instructions! Other instructions should be issued in accordance with Table 4 and notes thereto.

Note. Bit assignment is specified in Table 4. Upon completion of the above actions the display module switches to the operating condition with the preset parameters.

RAM allocation

The display module comprises 80-byte RAM at 0h–27h and 40h–67h addresses for the storage of data (DDRAM) displayed on LCD. The addresses of characters displayed on LCD are allocated as follows:

Character location #		1	2	3	.....	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
ADDRESS	1st line	0h	1h	2h	....	8h	9h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h	14h	15h	16h	17h
	2nd line	40h	41h	42h	....	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh	50h	51h	52h	53h	54h	55h	56h	57h

User-programmable characters

The display module comprises memory for the storage of patterns for 8 user-programmable characters (CGRAM). The codes for these 8 characters are listed in Table 5. Addresses of these character patterns lines are independent of addresses of displayed characters (located in a separate address space). They hold addresses 0h to 3Fh. Each character takes up 8 bytes (0h–7h, 8h–Fh, 10h–17h, ..., 30h–37h, 38h–3Fh). Enumeration of bytes goes in the order of top-to-bottom display on LCD (the first byte is the topmost, and the eighth byte is the bottommost). The last eighth line is used also for displaying the cursor (if an underline cursor is selected). In each byte only 5 LSBs are used (4, 3, 2, 1, 0), 3 MSBs (7,6,5) are arbitrary, as they don't affect displaying. Bit 4 corresponds to the left column of the character matrix, while bit 0 — to the right character column. See example in Table 3.

Table 3.

Character code	Address in the character generator		Values in the character generator	
7 6 5 4 3 2 1 0	5 4 3	2 1 0	7 6 5	4 3 2 1 0
0 0 0 0 0 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0
		0 0 1		1 0 0 0 1
		0 1 0		1 0 0 0 1
		0 1 1		1 1 1 1 0
		1 0 0		1 0 1 0 0
		1 0 1		1 0 0 1 0
		1 1 0		1 0 0 0 1
		1 1 1	* * *	0 0 0 0 0
0 0 0 0 0 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1
		0 0 1		0 1 0 1 0
		0 1 0		1 1 1 1 1
		0 1 1		0 0 1 0 0
		1 0 0		1 1 1 1 1
		1 0 1		0 0 1 0 0
		1 1 0		0 0 1 0 0
		1 1 1	* * *	0 0 0 0 0
		0 0 0	* * *	
		0 0 1		
0 0 0 0 0 1 1 1	1 1 1	1 0 0		
		1 0 1		
		1 1 0		
		1 1 1	* * *	

1st character pattern

Cursor position

2nd character pattern

Cursor position

* — the value doesn't affect displaying

Description of instructions

Table 4.

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution time
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears display and moves cursor to the leftmost position	1,5 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Moves cursor to the left position	40 µs
Entry Mode Set	0	0	0	0	0	0	0	1	ID	SH	Sets cursor to shift directions(ID=0/1—left/right) and enables display shift (SH=1) during write to DDRAM	40 µs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets LCD on (D=1) and selects cursor type(C, B), see Note 4	40 µs
Cursor or Display Shift	0	0	0	0	0	1	SC	RL	X	X	Shifts display or cursor (SC=0/1—cursor/display, RL=0/1—left/right)	40 µs
Function Set	0	0	0	0	1	DL	1	0	P	0	Sets interface data length (DL=0/1—4/8 bits) and character-generator page (P)	40 µs
Set CGRAM Address	0	0	0	1	ACG						Sets address for further operations (and moves cursor to that location) and selects CGRAM space	40 µs
Set DDRAM Address	0	0	1	ADD							Sets address for further operations and selects DDRAM space	40 µs
Read BUSY flag and Address	0	1	BS	AC							Reads busy flag and reads address counter contents	0
Write Data to RAM	1	0	WRITE DATA								Writes data to the active space	40 µs
Read Data from RAM	1	1	READ DATA								Reads data from the active space	40 µs

Note:

1. The execution time specified is max. You don't have to observe the execution time provided that the busy flag (BS) is read. As soon as BS=0, you can write the next instruction or data. If prior to instruction issue BS is not checked, the waiting time between instructions shall be longer than the execution time to ensure reliable operation of the display module.

2. When reading status bit no waiting time is needed.

3. Capital X — any value (0 or 1).

4. C and B bits in the 'Display ON/OFF control' instruction:

   C=0, B=0 — cursor off, blinking off;
   C=0, B=1 — cursor off, blink of cursor position (the entire character in cursor position is blinking);
   C=1, B=0 — cursor on (underline), blinking off;
   C=1, B=1 — cursor on (underline) cursor blink on (the only blinking).

Table 5. Page 0 built-in character generator.

Table 6. Page 1 built-in character generator.

Upper code digit character (hex)

Lower code digit character (hex)

Table 7. Pinout.

Pin	Symbol	Pin assignment
1	GND	Common pin (0V)
2	U_{CC}	Supply voltage (5V/3V)
3	U_o	Contrast adjustment
4	A0	Address signal — selection between transmission of data and instructions
5	R/W	Read/Write mode selection
6	E	Enable display access (and data strobe)
7	DB0	Data bus (8-bit operation mode)(LSB in 8-bit operation mode)
8	DB1	Data bus (8-bit operation mode)
9	DB2	Data bus (8-bit operation mode)
10	DB3	Data bus (8-bit operation mode)
11	DB4	Data bus (8-bit and 4-bit operation modes)(LSB in 4-bit operation mode)
12	DB5	Data bus (8-bit and 4-bit operation modes)
13	DB6	Data bus (8-bit and 4-bit operation modes)
14	DB7	Data bus (8-bit and 4-bit operation modes)(MSB)
15	+LED	+ of backlight power supply
16	–LED	– of backlight power supply

MT–24S2L LCD display module dimensions

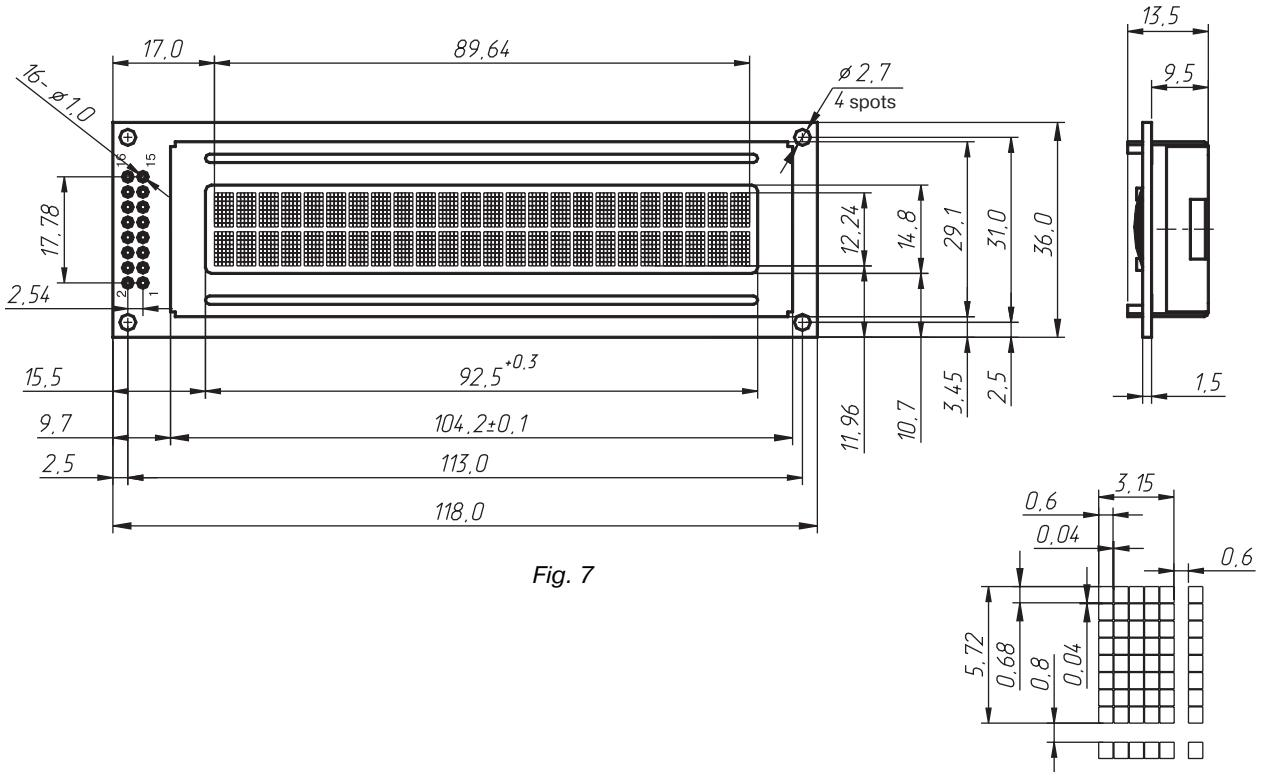


Fig. 7

Revision History

Document version	Date	Alterations	Page
1.0	06/18/2013	Revision 1.	

MELT Co.

Address and Contact details

26 Andronovskoye Chaussee, bld. 5, Moscow
Tel./Fax: +7 (495) 662–44–14 (multichannel)
e–mail: sales@melt.com.ru
http://www.melt.com.ru

Passed for printing on June 18, 2013. A4 format.
Printed in Russia.